ABSTRACT OF THE DISCLOSURE

A debugging interface includes a pair of decoders and an event history buffer coupled to the sequencer of a processor. The first decoder is coupled to the program counter of the sequencer and the Instruction RAM of the processor. The second decoder is coupled to the cause register of the sequencer and the event history buffer is also coupled to the cause register. The first decoder provides a three bit real time output which is indicative of the processor activity on a cycle by cycle basis. The three bit output indicates seven different conditions: whether the last instruction executed by the processor was an inc, an exception, an exception with no event history buffer entry, or a branch taken, whether there has been no instruction executed since the last clock cycle, and whether a jump was an immediate jump or a jump to a register. The event history buffer is loaded with more detailed information about the instruction last executed when the first decoder indicates that the last instruction was an exception or a jump to a register, and when there is a change in state of an interrupt line or an internal processor exception. An exemplary implementation of the debugging interface is embodied on an ASIC chip having three processors. Each processor is provided with a first and second decoders and a single event history buffer for all processors is provided on the chip.